REMARKS

The enclosed is responsive to the Examiner's Final Office Action mailed on December 16, 2009 and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114. At the time the Examiner mailed the Final Office Action claims 89-104 were pending. By way of the present response the Applicants have: 1) amended claims 89 and 91; 2) added new claims 105-109; and 3) canceled no claims. As such, claims 89-109 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now represented.

Allowable Claims

Applicants thank Examiner for the allowance of claims 101-104.

Claim Rejections

35 U.S.C. 103(a) Rejections

The Office Action rejected claim 89 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,740,357 (hereinafter "Gardiner") in view of U.S. Patent 5,781,750 (hereinafter "Blomgren"). Prior to addressing the rejection, Applicants would first like to thank Examiner for providing more details in the Response to Arguments section which have helped Applicants understand what the previous rejection was stating.

With respect to claim 89, the combination does not describe:

> A processor comprising:
> first logic to detect an error;
> second logic to attempt to correct a detected error;
> and
> a first interface to a first memory external to the processor that stores a set of procedures to access the processor across different processor implementations and at least a first software error handling routine to be invoked by

the processor via the first interface when the second logic cannot correct the detected error.

The combination does not describe "*a first interface to a first memory external to the processor that stores a set of procedures to access the processor across different processor implementations and at least a first software error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error*." The Office Action cites the combination of Gardiner and Blomgren as describing this limitation. Turning to the first paragraph of the rejection, it stated that Gardiner discloses:

> **A first interface to a first error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error** (From line 44 of column 6, "If the recovery is not successful, a fail response and error report (if applicable) is sent to the next higher level." Further, from line 55 of column 8, "In addition to the analyzer function 41 having access to lower level entities, the access function 43 allows management of the local level error handler 40 by a higher level entity 12. Some of this management of the local level error handler 40 includes reading and writing of a scratch pad function 42 that serves as temporary storage of error, state, and status information; access to and control of analyzer function 41 attributes, such as counters and error handling thresholds; switching the reporting function 44 to report to the tester 60 instead of to the fault handler 50, or to the next high level entity; and for diagnostic purposes, the higher lever entity 12 may change the reporting function 44 to report only to the tester 60 via the access function 43."). (emphasis added)

In the Response to Arguments section, it appears that this part of the rejection is directed solely at the interpretation that "Gardiner describes an interface to an error handling routine, but not necessarily to memory, for which Blomgren was brought in to teach." What was previously confusing was that the rejection, as written, appeared to state that Gardiner described everything which is simply not the case. Again, Applicants thank Examiner for clarifying in the Response to Arguments section. Looking at Gardiner, there are potentially several levels of error correction, however, there is no interface to memory and zero mention of any error handling routine stored in a memory.

Therefore, the Office Action "brought in" Blomgren to attempt to bridge the gap. However, there is nothing in the combination Gardiner and Blomgren to suggest that there is the claimed interface to memory wherein the memory stores a set of procedures to access the processor or wherein the memory stores an error handling routine. The rejection, as repeated by the Office Action, in part reads:

> **Although Gardiner does not specifically disclose a first memory that stores a set of procedures to access the processor and the first error handling routine (thereby making it software), memory to store code to access a processor is known in the art**. An example of this is shown Blomgren, from the abstract, "Emulation mode is entered upon reset, and performs various system checks and memory allocation. A special emulation driver is loaded in to a portion of main memory set aside at reset. Software routines to emulate the more complex instructions of the CSIC architecture using RISC instructions are also loaded into the emulation memory." A person having ordinary skill in the art at the time of the invention should have been motivated to have such memory and code because, from line 46 of column 3 of Blomgren, "it would be a tremendous competitive advantage to be able to run native x86 code on a RISC CPU". Further, such a component may function as a device in Gardiner's functional hierarchy, operating between the processor and whatever is attempting a natively access the processor. (emphasis added)

In the emphasized section, it is clear that the Office Action is not contending that Gardiner has a memory that stores the first error handling routine. What Applicants still do not understand is how the Office Action comes up with a combination that does meet this limitation. Blomgren apparently was brought in to teach an interface to memory, but not storing of an error handling routine. Why would the mere existence of an interface to memory in Blomgren (which Applicants contend does not even exist) suddenly in combination with Gardiner describe the limitation? Is there a hint that the memory could such a routine? No. Is there any other rationale for that to be the case such as those found in MPEP 2143? No. Simply put, there is no rationale for the combination to be made and the combination therefore would not describe what is being claimed. Moreover, Gardiner's system has an explicit way of functioning and there is no indication that making the

suggested combination of Blomgren and Gardiner would even work with a reasonable expectation of success.

Additionally, the Office Action states that "Blomgren, as cited, discloses procedures stored in a memory that allow a processor to be accessed." Blomgren, as cited, loads an emulation driver into main memory and routines to emulate CISC using RISC instructions are also loaded. However, emulation is simply the duplication of the functions of one system using a different system. It has nothing to do with access to a processor. Therefore, Blomgren's emulation is not a set of procedures to access a processor or a software error handling routine. The Office Action further notes that "It should also be noted that Gardiner's entity has procedures to access itself." While Applicants do not understand what that means (why would an entity have procedures to access itself?), it seems irrelevant to the issues at hand.

For at least these reasons, the combination does not describe what Applicants are claiming. Claims 90-92 are dependent on claim 89 and are allowable for at least the same rationale.

The Office Action rejected claims 90-92 under 35 U.S.C. 103(a) as being unpatentable over Gardiner and Blomgren as applied to claim 89 above, and further in view of U.S. Patent 5,594,905 (hereinafter "Mital"). Claims 90-92 are dependent on claim 89 and are allowable for at least the same rationale

The Office Action rejected claims 93 and 94 under 35 U.S.C. 103(a) as being unpatentable over Gardiner in view of Blomgren and Official Notice.

With respect to claim 93, the combination does not describe:

> A system comprising:
>
> a processor;
>
> a first memory coupled to the processor, the first memory to store at least a first firmware error handling routine to be invoked by the processor to attempt to correct a detected error when the processor cannot correct the detected error; and

a display coupled to the processor.

The combination does not describe "a first memory coupled to the processor, the first memory to store at least a first firmware error handling routine to be invoked by the processor to attempt to correct a detected error when the processor cannot correct the detected error" for reasons similar to those discussed above.

For at least these reasons, the combination does not describe what Applicants are claiming. Claims 94-100 are dependent on claim 93 and are allowable for at least the same rationale.

The Office Action rejected claims 95, 97 and 98 under 35 U.S.C. 103(a) as being unpatentable over Gardiner and Blomgren and Official Notice as applied to claims 93 and 94 above, and further in view of Mital. Claims 95, 97, and 98 are dependent on claim 93 and are allowable for at least the same rationale.

The Office Action rejected claim 96 under 35 U.S.C. 103(a) as being unpatentable over Gardiner and Blomgren and Official Notice as applied to claim 94 above, and further in view of U.S. Patent 5,787,095 (hereinafter "Myers"). Claim 96 is dependent on claim 93 and is allowable for at least the same rationale.

The Office Action rejected claims 99 and 100 under 35 U.S.C. 103(a) as being unpatentable over Gardiner, Blomgren, Official Notice, and Mital as applied to claim 99 above, and further in view of Official Notice. Claims 95, 97, and 98 are dependent on claim 93 and are allowable for at least the same rationale.

In light of the comments above, the Applicants respectfully request the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Dave Nicholson at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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